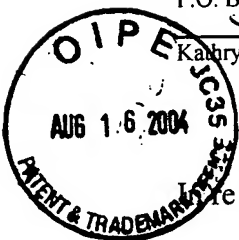


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Kathryn Marley



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Application of Inventor:

Jade M. Kizer

Application No. **10/645,201**

Confirmation No. **7115**

Filed: **21 August 2003**

Title: **Periodic Interface Calibration for High Speed Communication**

Group Art Unit: 2661

Examiner: Douglas W. Olms

CUSTOMER NO. 38342

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.56

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Enclosed with this statement is Form PTO-SB/08. The Examiner is requested to initial the forms and return them to the undersigned in accordance with M.P.E.P. 609.

Also enclosed with this statement is a copy of each cited document as required by 37 C.F.R. 1.98. The exception to this, in accordance with the 05 August 2003 Official Gazette Notice in which the USPTO waives the requirement for submitting copies of U.S. Patent and Publications for cases filed after 30 June 2003, is that copies of U.S. Patent documents and copies of U.S. Patent publications are not being submitted.

This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed before the mailing date of the first Office Action on the merits.

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (RBUS 1305-1). A copy of this authorization is enclosed.

Respectfully submitted,

Date:

10 Aug 2004

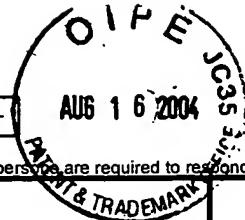
By:

Mark A. Haynes

Mark A. Haynes, Reg. No. 30,846

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Substitute for form 1449A/PTO			Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/645,201	
			Filing Date	21-Aug-2003	
			First Named Inventor	Jade M. Kizer	
			Group Art Unit	2661	
			Examiner Name	Douglas W. Olms	
Sheet	1	of	2	Attorney Docket Number	RBUS 1305-1

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A50	5,548,146		Kuroda et al.	08-20-1996	
	A51	6,377,640		Trans	04-23-2002	
	A3					
	A4					
	A5					
	A6					
	A7					
	A8					
	A9					
	A10					
	A11					
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		Application Number	10/645,201		
		Filing Date	21-Aug-2003		
		First Named Inventor	Jade M. Kizer		
		Group Art Unit	2661		
		Examiner Name	Douglas W. Olms		
		Attorney Docket Number	RBUS 1305-1		
Sheet	2	of	2		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C27	WIDMER, A.X., et al., "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM J. Res. Develop., Vol. 27, No. 5, September 1983, 440-451.	
	C28	BANU, MIHAI, et al., "TA 6.4: A 660Mv/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission," IEEE International Solid State Circuits Conference, 1993, 102-103, 270.	
	C29	ELDERING, CHARLES A., et al., "Digital Burst Mode Clock Recovery Technique for Fiber-Optic Systems," Journal of Lightwave Technology, Vol. 12, No. 2, February 1994, 271-279.	
	C30	CHANG, KEN K. Y., et al., "A 2 Gb/s Asymmetric Serial Link for High-Bandwidth Packet Switches," Hot Interconnects V, Stanford University, August 1997, 1-9.	
	C31	HU, TIMOTHY H., et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-μ CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, 1314-1320.	
	C32	KIM, SUNGJOON, et al., "An 800Mbps Multi-Channel CMOS Serial Link with 3x Oversampling," IEEE 1995 Custom Integrated Circuits Conference, 22.7.1-22.7.4.	
	C33	NAKAMURA, KAZUYUKI, et al., "A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock," 1998 Symposium on VLSI Circuits Digest of Technical Papers, 196-197.	
	C34	POULTON, JOHN, et al., "A Tracking Clock Recovery Receiver for 4Gb/s Signaling, Hot Interconnects '97, August 21-23, 1997, Palo Alto, CA, 1-13.	
	C35	DALLY, W, et al., "DIGITAL SYSTEMS ENGINEERING," Cambridge University Press, 1998, pages 447-449.	
	C36	CERISOLA, M., et al., "CORD - a WDM Optical Network: Control Mechanism Using Subcarrier Multiplexing and Novel Synchronization Solutions," Communications, 1995. ICC 95 Seattle, Gateway to Globalization, 1995 IEEE International Conference on , Volume: 1 , 18-22 June 1995 Pages:261 - 265 vol.1	

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